Cadence based Imlementation of Successive Approximation ADC using 45nm Cmos Technology

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Abstract: The Successive approximation ADC is best suitable for low power applications with moderate speed and simple design. This project describes the design of SAR architecture ADC with 4-bit resolution and clock frequency ranging from 20MHz to 1GHz. The architecture mainly consists of 4 blocks Sample and Hold (S/H) circuit, SAR Logic block, DAC and comparator. S/H circuit is used to hold the signal until the conversion is completed. In this project it is implemented using transmission gates and MIM capacitor. Comparator used in this project is an auto zeroed capacitor comparator, used to compare the analog input signal with the reference voltage generated by DAC. DAC, used her is R-2R DAC, which converts output from SAR Logic into analog signal. SAR Logic Block initially approximates the digital output and then corrects the output based on comparator output. Here each individual blocks are simulated separately using Cadence tool in CMOS 45nm technology. At the top level all the blocks are integrated and simulated with power supply of 1.1V. Power dissipation from the circuit is 0.108mW.

Introduction

The analog to digital converter is considered to be an encoding Device, where it converts an analog sample into a digital quantity with a prescribed number of bits. Numerous types of A/D converters have been designed for a wide variety of applications. There are 4 different types of architecture: pipeline, flash-type, successive approximation and over sampled ADCs. The type of the application largely determines the choice of the A/D converter technique. ADC has continuous, infinite value signal as its inputs, the important analog points on the transfer curve for an ADC are the ones that corresponds to changes in the digital output world. The most commonly used ADC among all ADCs types are Flash ADC and SAR ADC. Flash ADC is the fastest ADC among all the ADC, it converts n bits in single clock cycle. In order to achieve that speed, it requires more number of comparators, which results in high power dissipation. This is the main drawback of using Flash ADC. For the applications with low power consumption and moderate speed SAR ADC is the best ADC [1].

Literature Survey

From [3], two types of Data convertors are studied, i.e., ADC and DAC. Different types of ADC's like Flash ADC, SAR ADC, Delta sigma ADC, Servo tracking ADC etc. are studied and compared based on parameters like speed, power, resolution and complexity in design. Based on this comparison SAR ADC was selected for our design. In [1] the logic behind the working of SAR ADC was studied. From [2] R2R design and working was analysed and implemented the same in our design. From paper [5] the design of comparator i.e., auto zeroed capacitor comparator was taken for our design. In [4] the sample and hold circuit was studied and taken as reference for our design.From paper [6] the design of SAR Logic blockfor our design.

Block Diagram of SAR ADC

A simpleSAR ADCblock diagram is as shown in the fig. 1, it consist of 4 main blocks are Sample and Hold, Comparator, R-2R DAC and SAR logic.

Sample and Hold circuit

Sample and Hold circuit is used to provide a constant input voltage to ADC conversion. This circuit mainly has two operational modes; one is sample mode and another hold mode. In Sample mode the applied input voltage is sampled and capacitor will get charge to that voltage. In hold mode, capacitor value is retained until next sample value of input. Sample and hold is a simple circuit it consists of a switch which is connected parallel to the capacitor. It is also called as track and hold circuit. Then the switch is used to obtain the analog signal and capacitor is used to hold the sampled analog voltage value until the next clock cycle is applied [4].

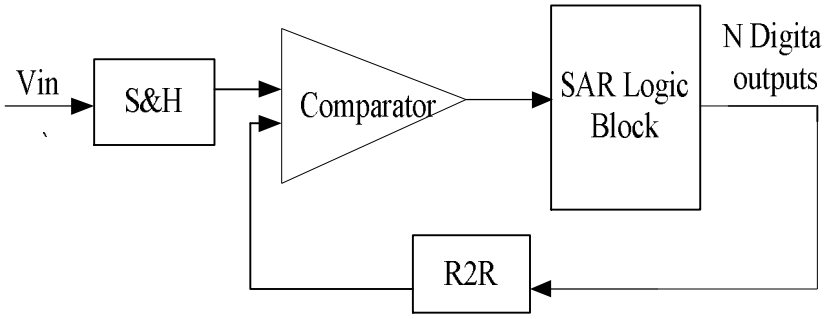

Fig.1: Block diagram of SAR ADC

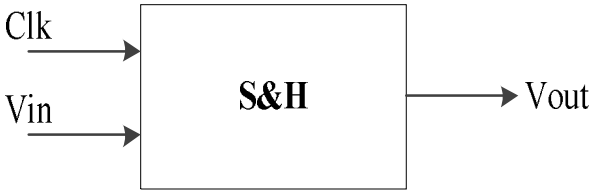

Fig.2: Block diagram of Sample and Hold circuit

The purpose of sample and hold circuits usually used in data converters i.e., Analog to Digital converter because in order to eliminate the noise in the input during the process of conversion. The analog signal is applied to the input of sample and hold and the output of the sample and hold is used to compare with the reference voltage produced by DAC and applied to the SAR logic block to perform the operation.

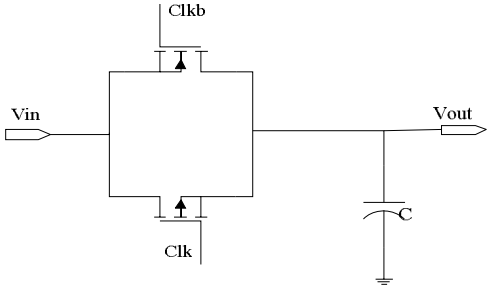

Fig3: Schematic of sample and hold

The continuously varying/changing analog signal is applied to the input switch, when the switch is closed the capacitor charges up to the value of the input analog voltage. When the switch is open, it holds the corresponding analog voltage across the output until the switch is closed for next sample of input voltage hence the name is called sample and hold.

Comparator

The analog Block in the SAR ADC is the Comparator. The actual conversion mainly depends on the output of Comparator. It compares DAC output and Sample and Hold circuit output and produces output in the form of pulses. Based on this output value the Approximated digital output is corrected. If Vsh < = Vdac, then Co = logic 0 and Vsh > = Vdac, then Co = logic1 hence comparator generates a logic output high or low based on comparison of the analog input with a reference voltage.Thecomparator used in this SAR ADC design is a switched capacitor type. The schematicswitched capacitor comparator [5] is as shown in Fig4.

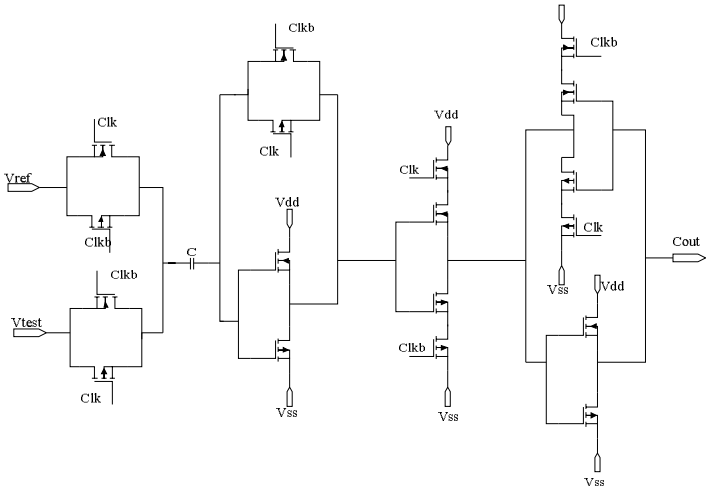

Fig 5:Schematic diagram of Auto-zeroed Capacitor Comparator

The detailed working of an Auto-zeroed Capacitor Comparator is as shown in the figure 2.7. It uses a CMOS inverter stage with three CMOS switches that is transmission gate –S1, S2 and S3 – and capacitor C, which samples the input signal, as well as the input offset voltage of the inverter. The CMOS switches are controlled by two complementary clock clk and clkb. During the first half clock cycle, when clk is high, switches S1 and S2 are both on and switch S¬3 is off. Switch S1 shorts the input and output of the inverter stage and charges one side of the capacitor C to bias voltage determined by the ratios of the devices in the inverter stage. The PMOS and NMOS devices, with their gate and drain tied are normally sized so that the bias voltage at the center node is approximately one-half of the positive supply voltage. The other side of capacitor C is connected to the input voltage Vin via switch S2. During this phase the comparator inverter is auto-zeroed to its toggle point by S1 open, the inverter becomes a gain stage and its gate floats around its toggle point. During the second half-clock cycle, clkb goes high and the reference resistor tap is now connected to the capacitor C through the switch S3. Any difference between the sampled input and resistor tap voltages will be amplified by the gain of the inverter stage, which has the same toggle point. This results in a force digital “high” or “low” output level. This level is captured in the latch on the trailing edge of clkb clock signal.

SAR Logic block

As the name itself indicates that it successively approximates the digital output bit by bit, starting from the MSB to LSB depends upon the clock signal. SAR ADC is successive approximation algorithm to converts the continuous changing analog signal input to the digital code. Based on the comparator value, it corrects its approximated digital output. This process is continued until all the bits are checked and corrected. Here we have considered the 4bit SAR ADC that is from D3-D0 hence N=4. For N bits it requires N+1 cycles to provide digital output for the corresponding sampled analog signals [6].

Table1:Overview of SAR working principle

Clock cycles(t)	Sampled analog signal in voltage	SAR output at different stages in the on conversion D3 D2 D1 D0	DAC output in voltage	Comparator output
1	11	1 0 0 0	8	1
2	11	1 1 0 0	12	0
3	11	1 0 1 0	10	1
4	11	1 0 1 1	11	1
5	5	1 0 0 0	8	0

SAR logic block which is proposed by Anderson consists of a Ring counter and a shift registers [6]. In the architecture it requires at least 2N flip flops are there for SAR control logic block.In this SAR logic block diagram includes 2N+2 flip flops

required to operate for N number of bits that is N=4 therefore we required 10 flip flops for the SAR operation is as shown in above figure 2.11. Here in this SAR logic block we have designed by considering the 3 different types of flip flop namely

- D flip flop with setb
- D flip flop with resetb
- D flip flop with set and resetb

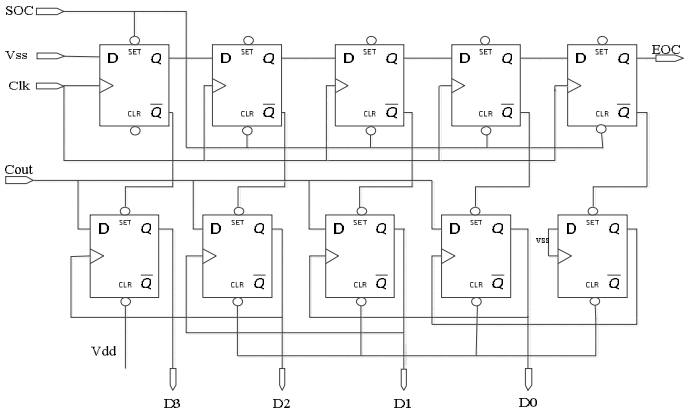

Fig6: SAR logic block

R-2R DAC

Digital to analog convertor is a type of Data convertor which converts digital signal into analog signal. In SAR ADC it is used to set a reference voltage for the comparator. The approximated/corrected bits from SAR logic Block is converted into analog and given to comparator as a reference voltage. Here we have considered the R-2R DAC. It is used to convert the digital values to the corresponding analog signal. The simple block diagram and schematic of R-2R DAC is shown below fig 2.7.By using the only two values of resistor R and 2R, a 4bit R-2R resistor ladder circuit along with the simple block diagram is shown in figure 2.15, d3 is MSB and d0 is LSB. The number of resistors required is 2N+1 there totally it requires 9 resistors. The principle used to solve this resistor network is Thevenin's equivalent circuit[2].

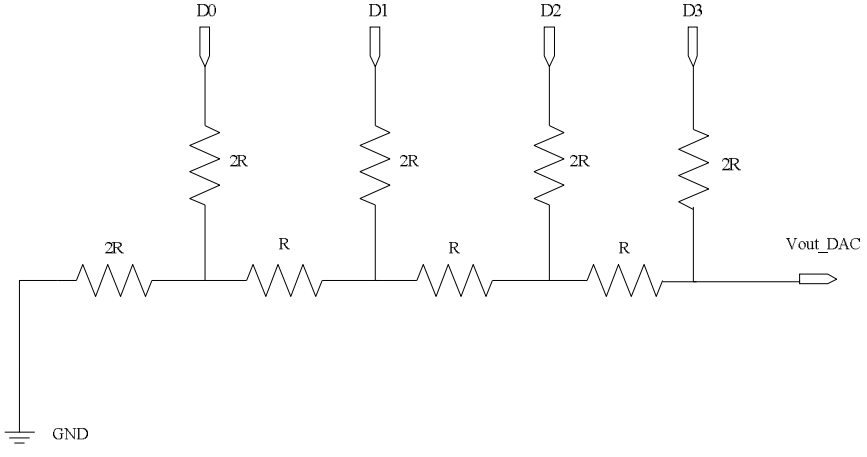

Fig8:Schematic of 4bit R-2R DAC

The digital inputs applied is either V=0 and V=V_{ref}. The R-2R network considered these digital bits to produce output voltage by using the weighted resistor R&2R. In this circuit depend upon the digital input is applied ex:0100, hence d3=0, d2=1, d1=0, d0=0, then output voltage is will have a corresponding stepped value in between 0 to V_{ref} minus the value of minimal step, corresponding to bit 0. The actual value of V_{ref} will depend on the type of technology used to generate the digital signal.

The output of digital value is obtained by

$V_{out} = V_{ref} * (Value/2^N)$

Where N= number of bits (i.e., N=4)
Value is from 0 to 15
V_{ref} =here it is 1.1 for 45nm technology.

Implementation of SAR ADC circuits using Cadence gpdk45nm technology

After implementing and simulating all the blocks individually, at the top level all are integrated as shown in the fig 9. The analog signal VIN is applied to sample and hold circuit. The output is given to comparator and another input for comparator is taken from R-2R DAC. The comparator compares both the value and produces output in digital pulses. This output is given to SAR based on which the SAR performs the conversion. The output from SAR logic is given to R-2R DAC. Final SAR ADC output is obtained by simulating the above Top Level Test bench and results are shown in the fig10. for the free running clock signal, when SOC goes low at the positive edge of the clock signal, SAR Logic block starts working by setting MSB and clearing other bits, then it is given to DAC and equivalent analog voltage is obtained and it is compared with Sample and Hold output. Depending on the comparison the comparator is obtained in form of digital pulses and given to SAR Logic Block to check whether the set bit in SAR is correct or not. This flow will be continued, hence for the analog input voltage the corresponding digital output is obtained by Successive Approximation method. The input specifications of top level are given in table1. Table 2 specifies the obtained results and output specifications.

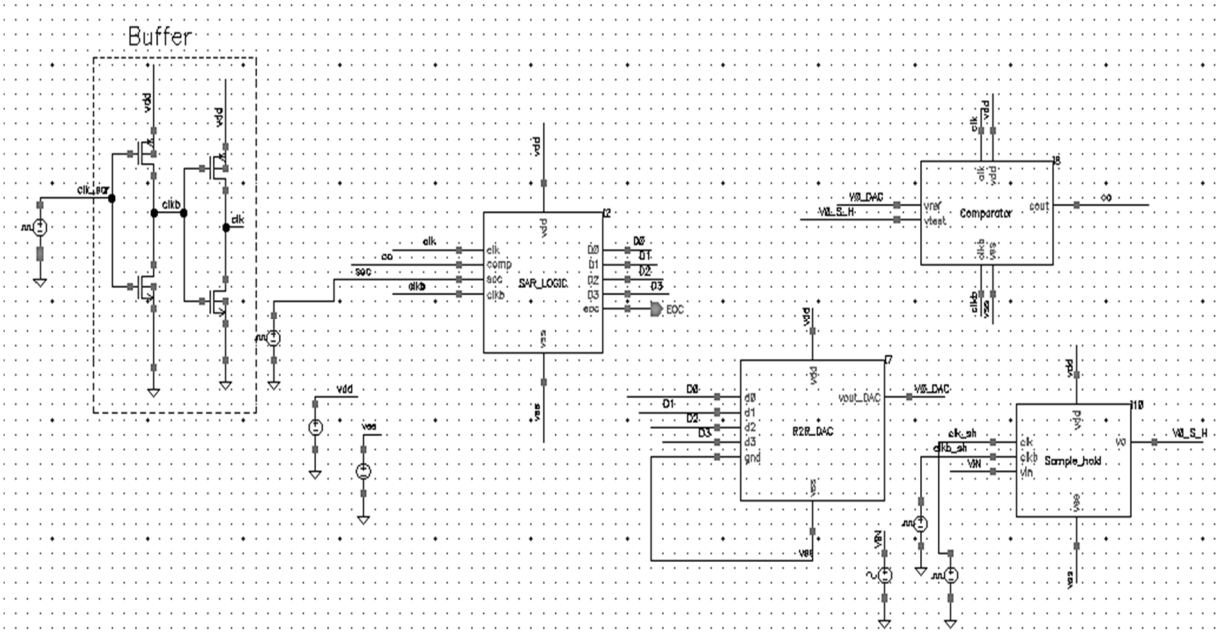

Fig9: Schematic implementation of top level SAR ADC in Cadence schematic editor

Table1: Input parameters and its specifications at top level

Parameters	Specifications
Input voltage(Vin)	Frequency: 2MHz, $Voltage_{(p-p)}$: 550mV
Clock signal (clk)	Range from 20MHz to1GHz (freq)
Clock signal for Sample and Hold circuit	One clock freq= 5*clk On time= 1/clk OFF time= 1/(4*clk)
SOC	One clock freq= 5*clk On time= 1/clk OFF time= 1/(4*clk)
Supply Voltage	1.1V

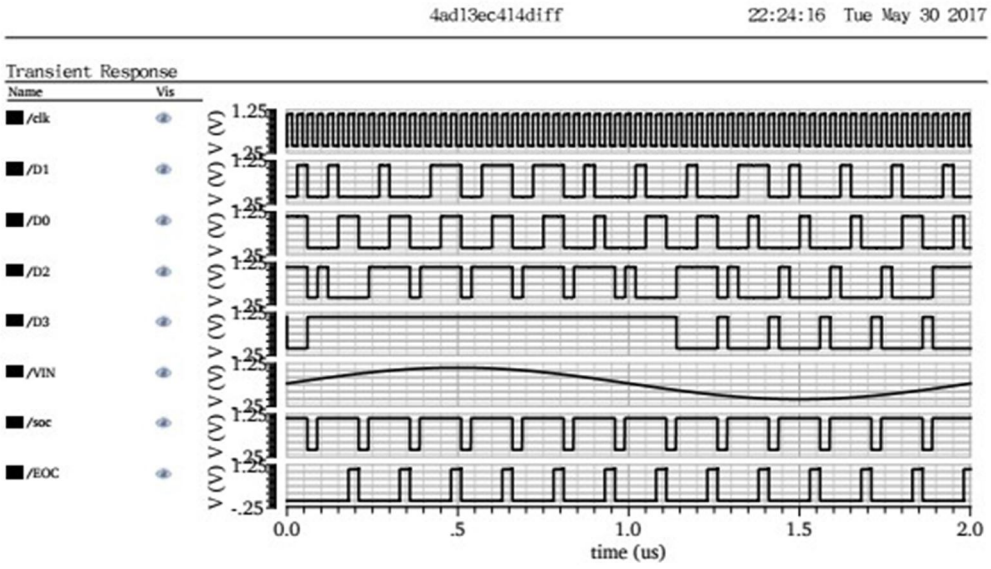

Fig10: Simulated waveforms of SAR ADC

Table 2: obtained results and output specifications

Parameters	Specifications
Technology	45nm CMOS
Supply voltage	1.1V
Speed	6.6GS/s
Resolution	4-bit
No. of transistors used	302
Clock range	20Mhz to 1Ghz
Power dissipation	0.108mW

Conclusion

In the above said design, a moderate speed 4-bit ADC is implemented which is very suitable for low power application and moderate speed wuth very simple design. The design uses N+1 clock cycles for N bits and supply power of 1.1V. total number of transistors used is 302. Since only one comparator is used the power consumption is very low. There is no external reference voltage given to the proposed architecture, since because the architecture itself generates the reference voltage by approximating the digital outputs by DAC.

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